In The Claims:

Claim 1 (Withdrawn) buried bit line formed in a substrate of a semiconductor device, comprising:

a shallow doped region, disposed in the substrate;

a deep doped region, disposed in the substrate under a part of the shallow doped region, wherein the shallow doped region and the deep doped region together serve as a buried bit line of the memory device;

Claim 2 (Withdrawn) The buried bit line of claim 1, wherein forming the shallow doped region and the deep doped region comprises:

forming a patterned mask layer on a substrate;

performing a first doping in the substrate not covered by the mask layer to form the shallow doped region, using the mask layer as a mask;

forming a liner layer with a predetermined thickness on at least a side surface of the mask layer; and

performing a second doping in the substrate not covered by the mask layer and the liner layer to form a deep doped region, using the liner layer and the mask layer as a mask.

Claim 3 (Withdrawn) The buried bit line of claim 2, wherein the mask layer comprises a photoresist material, polysilicon or a dielectric material.

Claim 4 (Withdrawn) The buried bit line of claim 2, wherein the liner layer comprises a high molecular weight material layer formed by plasma enhanced chemical vapor deposition.

Claim 5 (Withdrawn) The buried bit line of claim 2, wherein an implantation energy for forming the deep doped region is about 50 KeV to 120 KeV and an implantation energy for forming the shallow doped region is about 40 KeV to 80 KeV.

Claim 6 (Withdrawn) The buried bit line of claim 1, wherein dopant concentrations in the deep doped region and the shallow doped region are about the same.

Claim 7 (Withdrawn) The buried bit line of claim 1, wherein a dopant concentration in the shallow doped region is about $10^{21}/cm^3$ to $10^{22}/cm^3$

Claim 8 (Withdrawn) The method of claim 5, wherein a dopant concentration in the deep doped region is about 1021/cm3 to 1022/cm3.

Claim 9 (original) A fabrication method for a buried bit line, comprising:

forming a patterned mask layer on a substrate;

forming a shallow doped region in the substrate not covered by the mask layer;

forming a liner layer with a predetermined thickness on at least a side surface of the mask layer; and

forming a deep doped region in the substrate not covered by the liner layer and the mask layer, wherein the shallow doped region and the deep doped region together serve as a buried bit

Claim 10 (Currently amended) The method of claim 9, wherein the patterned mask layer is formed with a photoresist material, polysilicon or a dielectric material.

Claim 11 (Currently amended) The method of claim 9, wherein the liner layer is formed with a ~~high molecular weight material~~ polymer material.

Claim 12 (Original) The method of claim 11, wherein liner layer is reworked directly when deviations occur in a critical dimension after the liner layer is formed.

Claim 13 (Currently amended) The method of claim ~~9~~ 11, wherein the liner layer is formed by plasma enhanced chemical vapor deposition.

Claim 14 (Original) The method of claim 9, wherein the deep doped region is formed with an implantation energy of about 50 KeV to 120 KeV.

Claim 15 (Original) The method of claim 9, wherein the shallow doped region is formed with an implantation energy of about 40 KeV to 80 KeV.

Claims 16 and 24 (Cancelled)

Claim 25 (New) A method of fabricating a memory device, comprises:
forming a patterned mask layer on the substrate;

performing a first ion implantation using the patterned mask layer as mask to form a plurality of shallow doped regions in the substrate exposed by the patterned mask layer;

forming a liner layer with predetermined thickness on at least a side surface of the mask layer;

performing a second ion implantation using the patterned mask layer and the liner layer as mask to form a plurality of deep doped regions in the substrate under a part of the shallow doped regions, wherein the dopant concentrations in the shallow doped regions and the deep doped regions are about the same;

removing the patterned mask layer and the liner layer;

forming a plurality of insulation structures on the shallow doped regions;

forming a plurality of gate oxide layers on the substrate; and

forming a plurality of word lines covering a part of the insulation structures and gate oxide layers over the substrate.

Claim 26 (New) The method of claim 25, wherein the patterned mask layer is formed with a photoresist material, polysilicon, or a dielectric material.

Claim 27 (New) The method of claim 25, wherein the liner layer comprises a polymer layer formed by plasma enhanced chemical vapor deposition.

Claim 28 (New) The method of claim 25, wherein the deep doped regions are formed with an implantation energy of about 50 KeV to 120 KeV and the shallow doped regions are formed with an implantation energy of about 40 KeV to 80 KeV.

Claim 29 (New) The method of claim 25, wherein a dopant concentration in the deep doped regions and the dopant concentration in the shallow doped region are about $10^{21}/cm^3$ to $10^{22}/cm^3$.

Claim 30 (New) The method of claim 25, wherein the insulation structures is formed by a thermal oxidation process using a patterned hard mask layer.

Claim 31 (New) A method of fabricating a silicon nitride memory device, comprises:

forming a patterned mask layer on the substrate;

performing a first ion implantation using the patterned mask layer as mask to form a plurality of shallow doped regions in the substrate exposed by the patterned mask layer;

forming a liner layer with predetermined thickness on at least a side surface of the mask layer;

performing a second ion implantation using the patterned mask layer and the liner layer as mask to form a plurality of deep doped regions in the substrate under a part of the shallow doped regions, wherein the dopant concentrations in the shallow doped regions and the deep doped regions are about the same;

removing the patterned mask layer and the liner layer;

forming a plurality of insulation structures on the shallow doped regions;

forming a electron trapping layer containing a silicon nitride layer on the substrate; and

forming a plurality of word lines on the substrate.

Claim 32 (New) The method of claim 31, wherein the mask layer is formed with a photoresist material, polysilicon, or a dielectric material.

Claim 33 (New) The method of claim 31, wherein the liner layer comprises a polymer layer formed by plasma enhanced chemical vapor deposition.

Claim 34 (New) The method of claim 31, wherein the deep doped regions are formed with an implantation energy of about 50 KeV to 120 KeV and the shallow doped regions are formed with an implantation energy of about 40 KeV to 80 KeV.

Claim 35 (New) The method of claim 31, wherein a dopant concentration in the deep doped regions and the dopant concentration in the shallow doped region are about $10^{21}/cm^3$ to $10^{22}/cm^3$.

Claim 36 (New) The method of claim 32, wherein the insulation structures is formed by a thermal oxidation process using a patterned hard mask layer.

In The Title:

~~STURCTURE OF A MEMORY DEVICE AND FABRICATION METHOD THEREOF~~

METHOD OF IMPROVING DEVICE RESISTANCE